DBBC.2 MANUAL

ver.2.3

INDEX

Introduction

This document describes the DBBC system in the 2009 implementation. The main component parts are described in the functionality in order to allow the customer how to handle maintenance and troubleshooting of the system. No distinction is done between User Manual and System Manual and both types of information are reported embedded one to the other, leaving the relevant elements be hopefully more straightforward to be used.

The DBBC system is a general purpose instrument and it is well adopted as VLBI back-end just because during its development a standard VLBI terminal, as diffused around the world , was taken into account as element the new system had to emulate. This functionally alone could not justify the development process as it was expected to achieve more flexible performance. For this main reason the DBBC system should not be considered a copy of a MKIV back-end system and the main distinctions need to be kept in mind for an appropriate use of the very powerful system that allows to add to a radio-telescope equipment a very general purpose data processing element.

1. System Overview Description

A general description of the DBBC system is given in this chapter with the goal to give the customer the possibility to easily recognize the main parts with a distinction for functionality.

A general overview of the system is showed in the figure 1.1. It could be noticed as the different elements are disposed in a way that could simplify the maintenance operations, and help to create its own system is simplified manner.

A distinction has been done in order to define functional blocks. A list follow:

a) Mechanical Set

It includes all the mechanical parts, that are relevant for the proper functionality of the system.

b) Cooling Set

It includes the electrical and mechanical elements in charge for a proper cooling of the entire system.

c) Power Distributor

All the elements used for powering the DBBC electronics are kept under this definition, including the power supply for the PC Set.

d) PC Set

It's the group of parts that are adopted for managing the system and have a dialog with the external world.

e) Conditioning Module

The modules are the relevant interface between an analog source, like a receiver, and the system before the analog to digital conversion.

f) CaT

Two boards are in charge for generate all the relevant signals related to the Clock and Timing functionalities.

g) FiLa Boards

These boards are the digital edge interfaces between the external side and the DBBC main functional block.

h) ADB1 Boards

They represent the analog edge interface between the external side and the DBBC main functional block.

j) Core1 Boards

The processing elements in the DBBC Block.

k) Connection Set

It represent the entire group of cables that are used to route all the signals, in the analog or digital domain between one to the other element of the system.

l) Firmware Set

The collection of FPGA configuration files to be used in the Core Boards.

m) Software Set

The collection of processor files able to manage the entire system.

n) Doc Set

This document is part of the set that includes also all the information reported in the DBBC web site.

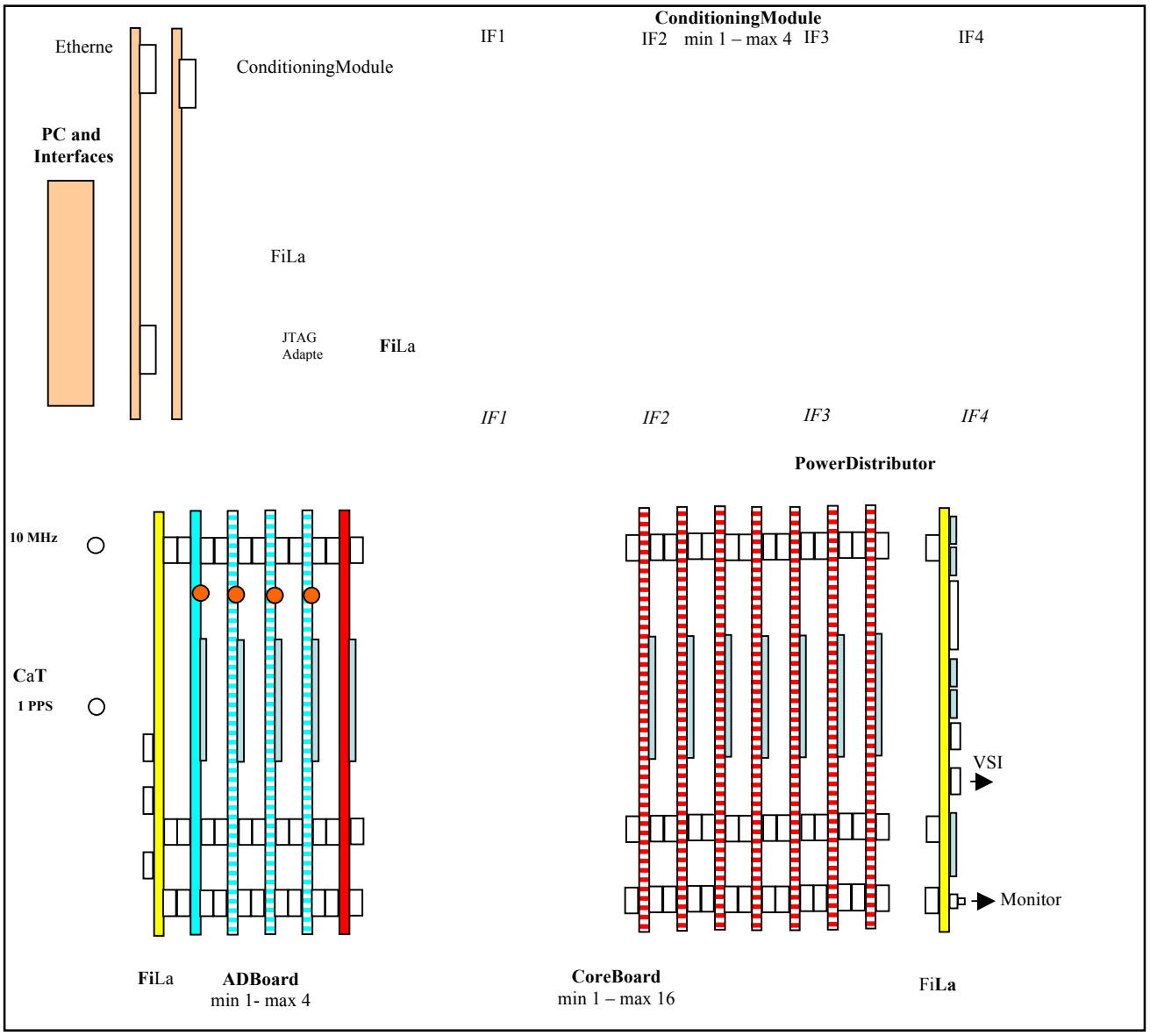

Fig.1.1 DBBC top view

2. Mechanical Set

2.1 Description

The DBBC is mechanically assembled in a 19 inch sub-rack box, 8 U height, 500 mm deep, so to include everything is necessary for a complete standard system. In the front panel, lower right side a blue led indicates when the main power switch is activated. In the rear panel mere elements are present for the connection. In the left lower side there are three switches, one big, two. The big one is just close to the mains connection. The 200VAC power cord should be there applied. It should be noticed as in the same block is present also a general protection fuse. The general switch when 'on' activate the cooling system in the DBBC mechanical box, giving also access to the further two smaller power switches, one for the general electronics, one for the internal PC system.

It can be noticed as the mechanics adopted is not composed by general purpose mechanical elements, but built from a company under drawing for the developed and dedicated parts. The thickness of the aluminum foils used is also conceived taking into account a robust and functional aspect.

The mechanical assembly is divided in virtually four parts internal to the box that can be considered dividing with two planes crossing one each other, one parallel to the up-down panels and one parallel to front-rear side panels. The figures 2.1 and 2.2 report the different sections.

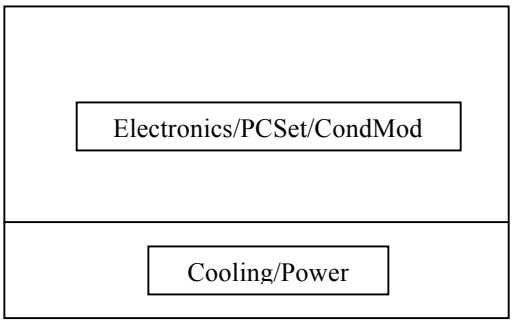

Fig. 2.1. Front view with two sections

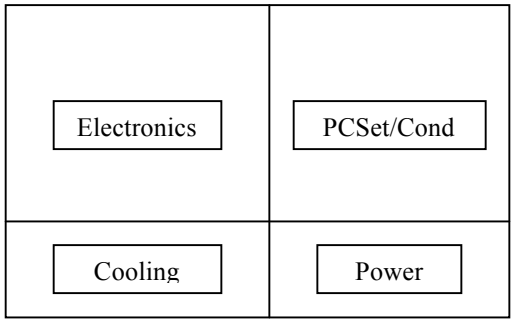

Fig. 2.2. Side view with four sections

The skeleton supporting the system is composed by the two lateral panels, in conjunction with six large bars joining the two panels. These alone constitute a structure where are mounted all the remaining parts. The lower front part is occupied by the fan closed in a box, supporting the upper electronics elements with a flexible structure in terms of positioning and number of DBBC boards in blocks. Several bar elements allow to place appropriately the boards still having the possibility to fix them in the needed position. A rear side half deep plane is used for supporting in the upper side the PC Set and Conditioning Modules, while in the lower side the three power suppliers used one for the PC Set, two for the electronics.

Two black panels with serigraphy are used in the front side. Under the upper front panel is mounted a second transparent Plexiglas panel, that can be used removing the first for having the possibility to look at the led indicators, still maintaining the appropriate cooling conditions with the air flow. Six panels are adopted in the rear side for the PC Set external connection, four Conditioning Modules, Power Distributor.

The upper and lower big panels cover the system and can be easily removed in case of need, because they do not support any other part.

In the fig 2.3 is showed the rear panel with the functional distribution of the modules placed in the rear side.

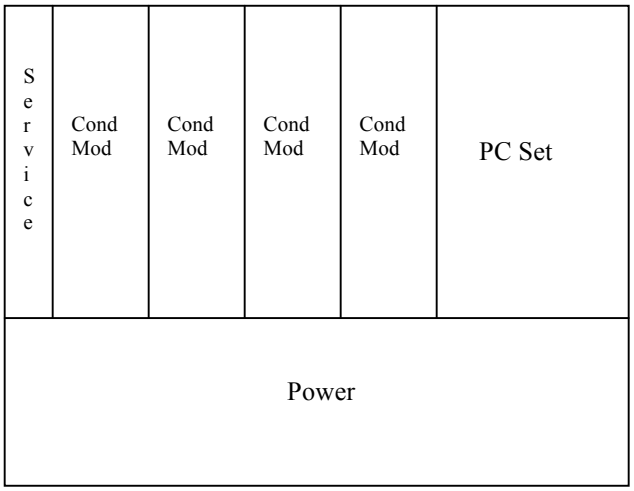

Fig. 2.2. Side view with four sections

3. Cooling Set

3.1 Description

The cooling system is an important element because it allows to properly assure a cooling air flow to the entire box, with a flow direction that is mandatory for keeping under proper conditions all the parts of the system. The air enter the system from the lower front panel, is captured by a tangential fan, then pushed to the half up side of the box, just under the functional DBBC boards block, then left to go to the rear side of the box, to a half upper and half lower when cooling is produced for the PC Set and to the Power Distribution Set. The fig 3.1 reports the air flow directions.

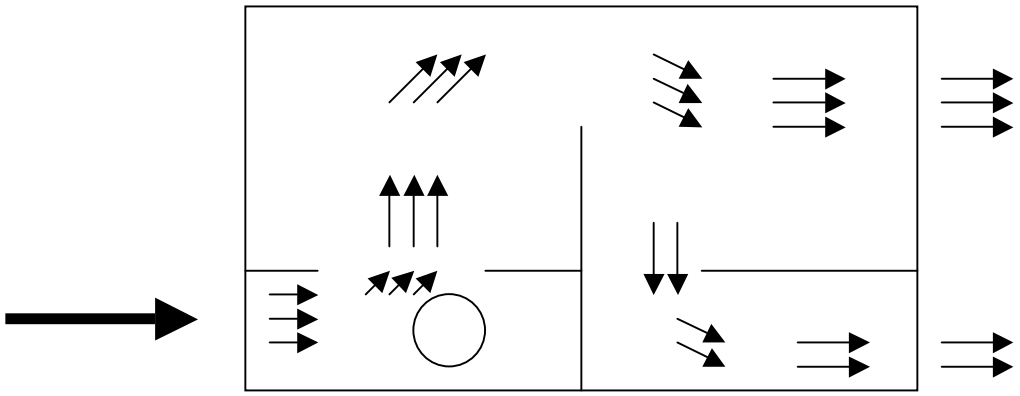

Fig. 3.1. The air cooling flow from a side view

3.2 Maintenance

Care should be taken to assure that the air flow is always appropriate and obstruction is in the air path. Periodic check should be made to the front panel thin net internal to the lower panel, and in case of accumulation of durst, it should be removed and cleaned with compress air.

A general removal of the internal dust is recommended once every 6 months with the help of compress air and vacuum cleaner.

4. Power Distributor

4.1 Description

The Power Distributor is the element that starting from the 220VAC mains produce the different voltages necessary for the different parts of the system. It is made by the following elements:

a) two identical units of switching power supply that produce each the power rails:
12V /13 A, +5V /40 A, +3.3V/40A, -12 V / 5A, total power 350W

b) one switching power supply for the PC Set, 350W

c) Power Distributor PCB, placed in the middle of ht box as separation between the analog and digital part, separating the PC Set and Conditioning Modules in one side and the digital electronics on the other side. This board receive the voltages from the switching power suppliers and generates what is necessary for the different boards of the DBBC stack in appropriate connectors placed in the top of the board. In particular in the pcb front panel it will be generated what necessary for:

c.1) one connector for CaT boards,

c.2) one connector for the first FiLa board

c.3) four connectors for ADB1 boards

c.4) sixteen connectors for Core2 boards

c.5) one connector for the last FiLa board

In the rear side of the pcb are present:

c.6) four connectors for powering the Conditioning Modules.

The Power Distributor PCB separates +5, +3.3V with appropriate filtering for the necessary different sections of all the boards and even in the same board for analog and digital sections, or even for different digital sections. Moreover in the pcb are produced such voltages that are not present on the switching power suppliers. This is necessary for the -5.2V used in the ADB1 boards, and for the 1.5V widely used as VCore in the Core1 boards. This last in particular requires large amount of current and a single additional

DC/DC converter is adopted for every Core1 board, each having the capability of 7A at 1.5V.

Single separate multi-wire cables are used to connect the Power Distributor PCB with every board in the stack, the CaT boards, and the Conditioning Modules.

In the tables below are reported voltages at the output of the Power Distributor PCB connectors.

	Pin1	Pin2	Pin3	Pin4	Pin5	Pin6
CaT	+3.3	+5.0	-5.2	+3.3	+12	GND
FiLa f/l	+3.3	GND	+3.3	GND	+3.3	GND
ADB1	+3.3	+5.0	+5.0	-5.2	GND	GND
Core2	+3.3	+3.3	+3.3	GND	GND	GND
CondMod	+12	-5.2	+5.0	+3.3	GND	GND

4.2 Maintenance

Check for proper voltage values once every year the output Power Distributor PCB connectors. Values are regular if in a range of +- 2% with respect to the nominal value.

5. PC Set

5.1 Description

The DBBC system has an internal industrial PC that is adopted for supporting a number of functionalities. In order to accomplish these tasks a single board PC is used on a small PCI bus together with three additional elements. Two of them are commercial boards from ADLink named PCI 7200 and PCI9111HR, the third is still a commercial element from Xilinx acting as JTAG interface.

Let see the list of tasks supported by the PC Set:

a) download of the Firmware Set loaded from the system disk (hard disk or flash) to the Core1 boards.

b) management of the settings of the Core1 firmware configurations and readings of the parameters.

c) program of the CaT synthesizer for the appropriate 1024 MHz system clock generation.

d) management of the settings of the Conditioning Modules and readings of parameters.

e) management of observative DBBC schedule.

f) Field System interface.

The single board PC is Pentium 4 based, operating at 3.0GHz, with a support of 1GB RAM. The operating system is Windows XP because not all the drivers of the used devices are available under a single Linux version or not available at all for Linux. The system disk is a 80GB hard disk, but in some systems is available a disk 4 or 8 GB flash memory. In the rear side of the system connections are possible for a keyboard, a mouse, a USB2 port, a monitor. A wireless keyboard and mouse is furnished with the system, operating at low frequency. It is responsibility of the user to decide to adopt or not such device for possible RFI reasons.

The PCI 7200 commercial board is able to guarantee IO at 32 bit on separated bus, so two cables connect such board with the first FiLa board, digital interface accessing point to the DBBC stack. All the dialogue, register setting, register reading with the DBBC Stack is realized through this channel.

The PCI9111HR commercial board is used to drive the Conditioning Modules. It is able to read a number of analog channels with 16-bit resolution and for such functionality adopted to read the IF Total Power signal as coming form the Conditioning Module in the selected total band. Moreover the Conditioning Modules require some register setting and for such reason is still used a digital interface bus in the PCI9111HR. A single flat cable is connecting the PCI board with the top side of the Conditioning Modules providing the interface communication channel.

The Xilinx download cable is used to quickly load the configuration files to the Core1 chain, still maintaining the possibility to access the single board, as a JTAG scheme and interface is adopted for such functionality. The connection speed is fixed at 12 Mbps, but could be increased up to 30Mbps. A wide level of flexibility is assured by this Boundary Scan connection because a number of internal tests can be realized in the single board where this could be worth to be done.

5.2 Maintenance

It is recommended to clean from the dust the processor fan and keep the processor area free from any object that could affect the correct cooling of the processor. The PC Set is mounted on a single mechanical block, so it can be easily removed from the DBBC box for cleaning or check reasons. The access is from the rear side of the system.

6. Conditioning Module

6.1 Description

The punctionality of the system is the following:

a) pre-AD conversion amplitude signal conditioning
b) pre AD conversion Nyquist band definition
c) 4 RF input selection
d) output level control
e) Total Power measurement control
f) 2.2 GHz bandwidth

The connection between the IF signals coming from the receiver to the DBBC system is realized by the Conditioning Module. In the rear side of the DBBC are placed four separated modules, one for each IF. Two input SMA connectors are present in the Conditioning Module and can be used for two different sources with a software selectable switch.

The selected signal is then routed after level adjustment to a set of filters, one from 10 to 512 MHz, the other from 512 to 1024 MHz. The edge frequencies are defined at -15 dB. A switch select the needed frequency band and finally the signal is routed to the output and to the total power measurement detector. Such circuitry produce a voltage level proportional to the power in the band and is available to the rear part of the module together with the signal to be routed to the ADB1 boards.

The system having a programmable attenuator and a total power measurement can realize a closed loop level control with the closure realized by a control software. Indeed the total power level is sent to the PCI9111HR, making part of the PC Set, where is converted in the digital domain at 16-bit and kept available for the IF control software.

The system bandwidth is form 10MHz up to 2.2GHz, and the maximum number of filters selectable by the control software is four.

6.2 Maintenance and calibration

The Conditioning Module doesn't need any particular maintenance, and the calibration of the Total Power measurement system is not normally required, with the exception of a post-repairing event.

7. CaT Set

7.1 Description

The Clock and Timing Set represent the elements generating the necessary clock and timing signals from the external reference clock and time data coming from an H-Maser. The system clock used for sampling and for generate all the further clock signals is a 1.024GHz, that is produced by multiplication from the reference 10MHz coming from the rear external Service panel. Such panel reports all the in and out signals in support of the system.

The Clock board of the CaT receive the external reference 10MHz at a nominal level of 0 dBm and reproduce a copy available in the Service panel. A pretty flexible PLL closure scheme is adopted to generate the 1.024MHz necessary as system clock. Indeed a VCO is phase locked in loop in a programmable fractional divider scheme in order to get the possibility to generate a wide number of possible useful clock values (es. 2^31Hz) with very good phase noise performance. Six single-ended SMA output connectors are available on the top of the board, the first four used for driving the four ADB1 boards, the second two used to drive the Timing board and a monitor connector in the Service panel. The board is mounted on a dedicated mechanical assembly to be fixed in the general DBBC rack together with the Timing board.

The Timing board receiving the external 1PPS, produces two copies, one for the PCI 9111HR board, one for the FiLa first board. Internally to the Timing board five differential high resolution 1PPS are generated, and four of them are routed to the four ADB1. These signals are used to synchronize the sampling in the four Ifs. The synchronization is performed with 1PPS pulses lasting one period of sampling clock, so in the standard case, the pulses are long 1/1.024x10^9 = 0.9765625 ns.

An additional small board making part of this set is the 1PPS-PCI adapter used to produce from a standard 1PPS, as normally present in a station, long like one clock

cycle of 5 MHZ (200ns), a 280 microsecond long pulse for software synchronization. The small board is attached on the PCI9111HR connector and support also the connection of the four analog levels coming from the Conditioning Modules.

7.2 Maintenance and calibration

No maintenance or calibration is required.

8. FiLa Boards

8.1 Description

The FiLa board is used is the first and last board in the DBBC Stack, with a number of different elements populating the board in the different positions. In both positions the FiLa boards represent the digital interface between the extern and the DBBC Stack.

The FiLa in the initial position perform the following tasks:

a) data I/O interface

b) JTAG interface

c) 1PPS input

The FiLa in the final position performs the following tasks:

a) double VSI interface

b) DA monitor

The first board is connected through two flat cables with the PCI 7200 that operates at TTL levels, while the DBBC Stack can accept a maximum of 3.3V. So a level conversion is applied to data from the PCI7200, while data to the PCI board can be accepted with the LVTTL levels so no conversion is performed. A small connector join the Xilinx download cable to the DBBC Stack trough the FiLa and the JTAG Boundary Scan protocols can be adopted for configuration downloads and the scanning of devices. Termination of the JTAG chain is realized in the last FiLa with a jumper. Whether additional element should be added to the JTAG chain, the jumper should be removed and the chain closed in the last element. The chain could be continued connecting from the last FiLa JTAG connector.

The last FiLa support the functionality of two independent VSI interfaces as DOM, with the two VSI connectors to be connected with a dedicated cable just on the

board. In case of critical or long connections an equalizer scheme could be activated. For normal length, up to 2 m cables, no equalization is normally necessary.
A digital to analog converter is used to produce analog representation of a digital 12-bit monitor data. Not all the FPGA configurations support such functionality that could be very useful for debugging purposes. The analog output from the DA converter can be single-ended or differential and is routed to external Service panel.

8.2 Maintenance and calibration

No maintenance or calibration is necessary.

9. ADB1 Board

9.1 Description

The ADB1 Board is the analog interface of the DBBC Stack. It's able to produce a 8-bit representation of the input analog signal, that can be single-ended or differential. The board presents four connectors in the top side, two for differential clock, two for differential input signal to be sampled. In the normal conditions single-end inputs are adopted, and the negative unused input should be terminated with a SMA 50 ohm load.

The front edge of the board has two additional connectors used for a differential reset coming from the Timing board. This signal is used to synchronize all the ADB1 boards of the stack.

The sampling clock is 1.024 GHz and is routed to the MAX108 device that produces a digital 8-bit representation of the analog input signal. The input band is pre-selected by the Conditioning Module in the ranges 10-512 MHz and 512 – 1024 MHz so that any ambiguity is avoided. In order to slow-down the clock frequency to properly insert data in the HIS bus a demultiplexed representation in two bus is produced and the data represented in DDR. Clock propagated through the HIS bus is then 256 MHz so as the maximum spectral contend in the data path. Logic level is LVPECL operating at 3.3V. For a general use of the ADB1 board several jumpers are present, but no modification is generally necessary with respect to the configuration set at the factory.

8.2 Maintenance and calibration

No maintenance or calibration is necessary.

10. Core2 Board

10.1 Description

The Core2 board is the processing element of the data sampled by the ADB1. A configuration file is loaded to the programmable device through a JTAG connection and when the device is programmed a green led placed on the front edge will light. There are two groups of leds: sixteen green leds from the top side and four in the lower side. The meaning of the first group of leds is shown in the table 10.1.

1	DAC monitor clock
2	DAC enable
3	BBC0 overflow
4	BBC1 overflow
5	BBC2 overflow
6	BBC3 overflow
7	10KHz retuning enable
8	80 Hz continuous cal enable
9	Bwd code bit2
10	Bwd code bit1
11	Bwd code bit0
12	1PPS sync enable
13	Board Write Enable
14	DCM2 Lock Status
15	DCM1 Lock Status
16	1PPS

Table 10.1. Core1 Led indicators, upper group, all green

NOTE:

bwd code		
000	32MHz	@ 64 MHz clk (not yet implemented)
001	16 MHz	@ 32 MHz clk
010	8 MHz	@ 32 MHz clk
011	4 MHz	@ 32 MHz clk
100	2 MHz	@ 32 MHz clk
101	1 MHz	@ 32 MHz clk
110	0,50 MHz	@ 32 MHz clk (not yet implemented)
111	0,25 MHz	@ 32 MHz clk (not yet implemented)

The definition of the second group of leds is indicated in the table 10.2

1	Device configured, green
2	2.5V Vcco, yellow
3	1.0V Vcore, yellow
4	2.5V Vaux, yellow

Table 10.2. Core1 Led indicators, lower group

In a normal working state it should be found on: the leds indicating the bandwidth of the down converter, both leds indicating the correct lock status in the DCM1 and DCM2, 1PPS led pulsing at the rate of one pulse per second, the configuration of the device, yellow leds indicating the correct status of the voltage rails.

Data are available on the HIS bus and after transit to the FPGA are available to the HSIR bus for the following elements in the chain. Data converted are available on the HSO bus, and the proper cascade of the stack is assured with the HSOR bus. All the auxiliary signals for communication, monitoring, service, programming re realized in the third bus, the CCM/CCMR.

The FPGA device requires an important cooling so a heat sink cooler is placed on the top side of the device. Air flow is guaranteed by the lower side of the stack. No obstruction should be placed in the normal air path.

10.2 Maintenance and calibration

In normal conditions no maintenance or calibration is necessary.

11. Connection Set

11.1 Description

The set includes all the cabling necessary to route the signals from one board to the other or between input panels or output VSI connections. Everything is included and distinction can be done between RF connections and digital cables. The input signals from the receiver are directly routed without cabling to the Conditioning Modules, so that no cable is involved. The rear connector panel is instead connected to the different sections using small SMA pre-cabled cables, so a all the clock and analog signal distribution to the ADB1 boards. Digital cables include the connections between the PCI boards and the FiLa first and the Conditioning Modules. VSI output is using two cables directly joining the internal FiLa last to the user device (e.g. MK5B/B+).

11.2 Maintenance and calibration

No maintenance or calibration is required.

12. Firmware Set

12.1 Description

A number of configuration files is necessary for the proper working status of the system. Each Core board has its own set with a different file for each bandwidth supported. At the time of system configuration a file contains the boards present on the DBBC Stack and the file to be downloaded for the particular board in the stack. A modification in any Core modification requires the reconfiguration of the entire set of boards. This takes about 30 sec and it's realised at start-up time and after a system command requiring a modification in one or more Core boards.

12.2 List of configurations files

For any board, indicated with Y, it's at present available the following list of files. The actual file name will show the Core personality instead of Y, that ranges between 1 and 16.

dbbc2_4ch_U.bit (tunable, all the bands)

dbbc2_poly.bit (polyphase filter)

The files are placed in the directory c:\DBBC_conf\FilesDBBC

Additional configuration files will be added at the time of their development completion.

13. Software Set

13.1 Description

The DBBC Software Set is at present running under Windows XP due to some incompatibility between drivers operating in the system under different version of Linux. As soon as it will be available a common Linux release for all the involved drivers, it will be possible to adopt Linux operating system for those stations that would require this.

The main program to be used for standard operations with the DBBC is "DBBC Control". Running this software it will become available a console able to accept commands and to show output response. No aditional software is to be run, otherwise a conflict between different programs could occur in common resources. A socket is available for having the possibility to run the system under a remote control, as it could be the Field System. At presnt is planned to develop a class of FS station commands able to communicate through this socket with the “dbbc control” program.

A file named "dbbc_config_file.txt" (in the directory c:\dbbc_conf) is to be configured in advance to run the control software to take care of the status of presence of boards in the DBBC Stack, and to set the initial conditions of the system in terms of bandwidth and frequency settings. Any additional modification in a single bbc will modify the status of the control file, that so will maintain the last settings for a further reinizialization of the system. A typical content for this file is the following:

1 dbbc2.bit 100.00 4
1 dbbc2.bit 140.99 4
1 dbbc2.bit 170.99 4
1 dbbc2.bit 230.99 4
1 dbbc2.bit 340.99 4
1 dbbc2.bit 420.99 4

1 dbbc2.bit 470.99 4

1 dbbc2.bit 490.99 4

1 dbbc2_.bit 192.99 4

1 dbbc2.bit 207.99 4

1 dbbc2.bit 217.99 4

1 dbbc2.bit 247.99 4

1 dbbc2.bit 267.99 4

1 dbbc2.bit 272.99 4

1 dbbc2.bit 100.99 4

1 dbbc2.bit 100.99 4

each row representing one bbc. The first parameter can be 0 or 1 depending on the presence of a Core2 at an adddress between 1 and 16, the second parameter is the configuration file to be loaded, the third the frequency setting, the fourth the bandwidth.

Additional programs available only for test reasons and not to be run while "dbbc Control" is taking the control of the system are:

1) “agc_if “ it is used to manually set and monitor the status of the Conditioning Modules present in the system.

2) “ad9858” used to set the system clock to 1024MHz.

3) “test_poly16” to run the polyphase filter configuration

14. DBBC Command Set

Description

This chapter describes the basic commands the DBBC is able to recognize with the control console. The structure and the meaning of the different commands is Field System based, so to simplify the dialogue with the FS and minimize efforts on the FS side. Any commands sent to the interpreter from the DBBC console is then identical to the command sent from the Field System environment. Similarly output information issued by any command are reported in FS style.

List of commands

At present 10 commands are defined for the main functionalities:

1)

DBBCnn = freq, IF, bwdU, bwdL, gainU, gainL, tpint
(DownConverterConfiguration)

where

nn => 01, .. ,16 indicates the number of CoreModule;

freq => is the base band frequency in MHz, in the range 0010.000000 - 2,048.000000;

IF => A or B or C or D. Any Core2 is connected to a band in the standard communication so this value is only informative.

bwdU => band width of the upper side, in MHz;

bwdL => band width of the lower side, in MHz;

bwdL and bwdU are always the same in a single bbc.

gainU => gain of the upper side in the range 0 - 255, step 1

gainL => gain of the upper side in the range 0 - 255, step 1

this values could normally kept to 1 as the magnitude bit is controlled with a dinamic threshold.

tpint => total power integration time in seconds, in the range 1 - 60, step 1
(1 sec implemented at present).

DBBCnn

reports the setting of the CoreModule nn, including cal tone off.

DBBCnn/freq,IF,bwdU,bwdL,gainU,gainL,tpU/calon,tpL/calon,tpUcaloff,tpLcaloff

2)

DBBCIF(A,B,C,D) = input_ch, gain, filter

where

input => input channel of the four possible (1,2,3,4) .

gain => the gain of the channel is set in manual mode if a number is indicated in the range -16 to +16 dB, step 0.5 dB. If AGC is indicated the gain is automatically set so to satisfy the optimal level for the analog to digital converter.
filter=> 2 (10-512 MHz), 1 (512-1024 MHz), 3 (ext 1), 4 (ext 2)

DBBCIF

reports the settings of the IFs modules.

3)

DBBCFORM = VSI1 mode, VSI2 mode

where

VSI1/2mode => is the mapping of the 64 channels in the VSI1/2 interface. Possible predefined values are: GEO, ASTRO.

DBBCFORM

reports the settings of the VSI output mapping.

4)

DBBCMON= bnn[u|l]

set the Digital to Analog Channel source.

nn => 01,2,3 indicates the number of band;
u/l => upper or lower side band

DBBCMON

reports the Digital to Analog Channel source.

5)

DBBC_CAL_IF

reports the entire system total power and gain settings in the IF units. The output is:

DBBC_CAL_IF=tp_ifa, gain_ifa, tp_ifb, gain_ifb, tp_ifc, gain_ifc,, tp_ifd, gain_ifd
Not yet active

6)

DBBC_CAL_CH

reports the entire system total power and gain settings in the converted channels. The output is:

DBBC_CAL_IF=tp_l1, gain_l1, tp_u1, gain_u1, tp_l2, gain_l2, tp_u2, gain_u2, ..., tp_l16, gain_l16, tp_u16, gain_u16
Not yet active

7)

PPS_SYNC

Synchronize to external 1pps

8)

DBBCGAIN=dbbcnn,gainU,gainL

Adjust gain level
dbbcnn = 1-16
gainU = 0 - 255
gainL = 0 -255

9)

RESETALL

System reset

10)

RECONF

System reconfiguration

15. Schematics Drawing *In preparation*

15.1 Connection Set

15.2 Power Distributor

15.3 Conditioning Module

15.4 CaT Set

15.5 FiLa

15.6 ADB1

15.7 Core1

16. Firmware _4ch register description (dbbc2.bit)

Register (WD26 - WD22)	DataW (WD15 - WD00)	DataR (RD32 -RD00)	Meaning
0x0	NA	rd15-rd00	statistics output L
0x0	NA	rd31-rd16	statistics output U
0x0	wd01-wd00	NA	statistics selection 0x0 = MU - ML 0x1 = MU - SL 0x2 = SU - ML 0x3 = SU - SL
0x1	NA	rd15-rd00	Total Power L / calon
0x1	NA	rd31-rd16	Total Power U / calon
0x2	wd07-wd00	rd07-rd00	amplification L
0x2	wd15-wd08	rd15-rd08	amplification U
0x3	wd03-wd00	rd03-rd00	DA monitor selection 0x0 = na 0x1 = na 0x2 = U 0x3 = L 0x4 = MU 0x5 = SU 0x6 = ML 0x7 = SL 0x8 = Input data phase 0 0x9 = DDS cos phase 0 0xA = Mixer out I phase 0 0xB = Poly out Q 0xC = 1:4 out Q 0xD = Q out 0xE = I out
0x4	wd-15-wd00	rd15-rd00	Phase Offset
0x10	wd-15-wd00	rd15-rd00	VSI1 high output selection NA
0x11	wd-15-wd00	rd15-rd00	VSI1 low output selection Geo track assignment= 0

			Astro track assignment=1 Pattern = 2
0x12	wd-15-wd00	rd15-rd00	VSI2 high output selection NA
0x13	wd-15-wd00	rd15-rd00	VSI1 low output selection Fixed = 0|1 Pattern = 2
0x14	wd-15-wd00	rd15-rd00	Phase increment high
0x15	wd-15-wd00	rd15-rd00	Phase increment low
0x16	Any	NA	Phase increment load
0x23	wd15-wd0	rd15-rd0	General control 1pps out selection bit0 0 = 1pps 1us ?? 1 = 1pps 32 ?? Total power mode bit1 0 = normal 1 = cont. cal 10KHz DDS reset bit2 0 = off 1 = on DAC board out (only write) bit3 0 = off 1= on DCM256 status (only read) bit3 0 = unlock 1 = lock DAC clock inv (only write) bit4 0 = inverted 1 = not inverted DCM128 status (only read) bit4 0 = unlock 1 = lock lPPS tuning load (NA) bit5 0 = disabled 1 = enabled bit6 NA bit7 NA bit8 NA

			bit9 NA DAC Monitor clock set bit10 0 = 128 MHz 1 = 32 MHz 1PPS sync bit11 0 = no ext 1pps sync 1 = ext 1pps sync
0x24	NA	rd15-rd00	Total Power L / caloff
0x24	NA	rd31-rd16	Total Power U / caloff
0x28	wd02-wd00	rd02-rd00	Band Selection 0 = 32 MHz (NA) 1 = 16 MHz 2 = 8 MHz 3 = 4 MHz 4 = 2 MHz 5 = 1 MHz 6 = 05 MHz (NA) 7 = 025MHz (NA)
0x29	wd11-wd00	rd11-rd00	Magnitude threshold U
0x30	wd11-wd00	rd11-rd00	Magnitude threshold L
0x3E	Any	NA	DDS reset
0x3F	Any	NA	DCM reset