DBBC – A Flexible Environment for VLBI and Space Research: Digital Receiver and Back-end Systems

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Abstract. The Digital Base Band Converter project produced a general method and a class of boards giving the possibility to build a general purpose radio system for VLBI or single-dish observational activities. Moreover it is evident as disposing of elements able to operate in a frequency range of few gigahertz, the same parts can be adopted for the direct sampling of radio frequency bands, and not only for intermediate frequency stages. Such approach suggests the realization of what can be defined a 'digital radio system', where such definition would include receivers with conversion not realized with analogue techniques, while still maintaining only amplification stages in the analogue domain in order to satisfy requirements for the analogue to digital conversion unit.

This paper presents a description of the elements developed in the DBBC project, with their use in different environments, in order to realize different instruments. The flexibility of the system is then evident because an appropriate distribution and assembly of parts is able to satisfy more requirements.

The description includes also the upgrade program where new elements with improvements are introduced for additional functionalities and optimization of the general performance.

Keywords. Digital radio, digital back-end, FPGA.

1 Introduction

The DBBC system is a complete environment able to handle data processing for a variable number of radio frequency bands in order to produce a very general data output under different types of physical supports.

It is showed in the bibliography the evolution of the development that has been realised as an European VLBI Network project.

At the present time few other similar developments are under way, with pretty different elements in the architectural aspect. Indeed what is still keeping unique such project is the flexibility in joining different elements for getting a variable number of radio bands available for producing a large number of high data rate output signals. Such variability, that is reflected in an appropriate use of elements with their related cost, produce an high degree of flexibility.

The different elements can be placed in a multitude of hardware architectures, that adding the flexibility due to the FPGA elements in terms of 'internal' hardware realization, allows to achieve a very high degree of freedom for producing data processing of the signals detected by the receivers placed in the radio telescope.

Example of implementation are pointed-out in terms of different flavours of digital back-ends and digital receivers.

2 System components

2.1 The ADBoard1

An analogue signal coming from the receiver in order to be processed in numerical format needs to be converted in the digital domain. To realize such functionality the ADBoard1 is adopted.
Input and clock signals can be entered as single-end or differential. Moreover a differential reset input is available to be used to synchronize more boards when operating in the same environment. A picture of this system component is showed in the fig.1.

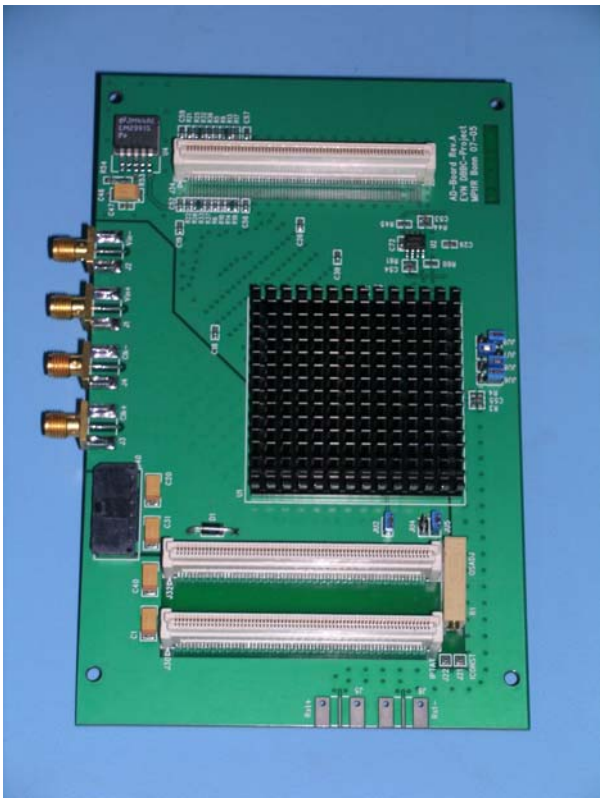

Fig. 1 Analog to digital conversion board ADB1.

The ADB1 is producing a digital representation of an analog signal entering the system up to a maximum frequency of 2.2 GHz, sampled at a maximum rate of 1.5 GHz with a 8-bit representation. In order to reduce the output data rate a 2x8-bit de-multiplexed version of two consecutive samples is produced in double data rate at a quarter of the sampling frequency. Additional functionalities are possible to take into account possible voltage offset present within the analog signal, so as different representation schemes.

2.2 The Conditioning Module

The analogue signal as coming from the receiver is not in general appropriate to enter the ADB1 because more elements need to be properly taken into account. Indeed the amplitude should be limited in order to avoid any over range that would introduce additional unwanted noise to the proper noise band. In the same time levels should be not too low so to optimize the signal representation in the conversion domain. In terms of frequency domain the AD device is able to sample data in multiple adjacent Nyquist zones, so the effective sampling frequency will be a limitation for the instantaneous bandwidth while maintaining the possibility to explore different regions of the spectrum for multiple higher frequency portions of such bandwidth. Such opportunity obliges to define which Nyquist zone to address to the AD to avoid superimpositions of simultaneous portions of the entire band satisfying the same requirements, with introduction of unwanted additional noise to the wanted part of spectrum.

A total power measurement needs to be available to the user for several reasons, such as real measurement for scientific purposes, signal level control, automatic gain control.

To accommodate all these functionalities the Conditioning Module has been developed able to take care of such aspects. An image of the first version is showed in the figure 2.

This unit is able to operate in the range 0.01-2.20 GHz as required by the ADB1 and can support a selection of one between four input channels. An active amplitude control in the range +-16dB assures

Fig. 2 Conditioning Module

a proper level control for the ADB1 and a selection is possible between four band definition filters, inserted in such unit.

Total power measure is available in the entire range and readable trough a digital interface, used also for all the other functionalities required to have a control related to the PCSet, a computer system, part of the DBBC components.

2.3 The CoreBoard1

Data coming from a maximum of four ADB1 boards are available to the processing elements, named CoreBoard1. A number of such boards can share the same group of sampled data, to produce a number of 64 processed channels. The output data channels could on the other hand be produced by different groups of sampled data, giving the possibility to produce a mix of channels coming from more than 4 input analogue channels.

The processing board adopts a large FPGA and is showed in the figure 3. With its the very general structure it's possible to process data injected into the board in a really great numbers of modes. So the output channels produced by one or more of such board will follow the mathematical sequence of operations internally programmed.

An output bus is carrying the 64 differential data channels, related clock and timing signals, while a further bus is adopted for service functionalities, like the dialogue with the PCSet, Jtag programming chain, digital to analog monitoring channel, an so on.

2.4 FiLa Board

The First/Last board of the system is named FiLa Board and accomplishes all the functionalities that are related to the communication with the external world. So the first board is able to act as a link between the PCSet and the elements of the system, to connect the Jtag programming interface, to insert 1PPS timing signals and other ancillary control functions. The last board is supporting two VSI interfaces with equalization control for adapting particularly long cables, includes a DA converter for monitoring functions, and support Jtag additional elements in the chain. An image is shown in figure 4. A set of external connections is available in order to support the monitoring of system 1PPS and the 80Hz synchronization signal for continuous Tcal measurements.

Fig. 3 The processing board CoreBoard1.

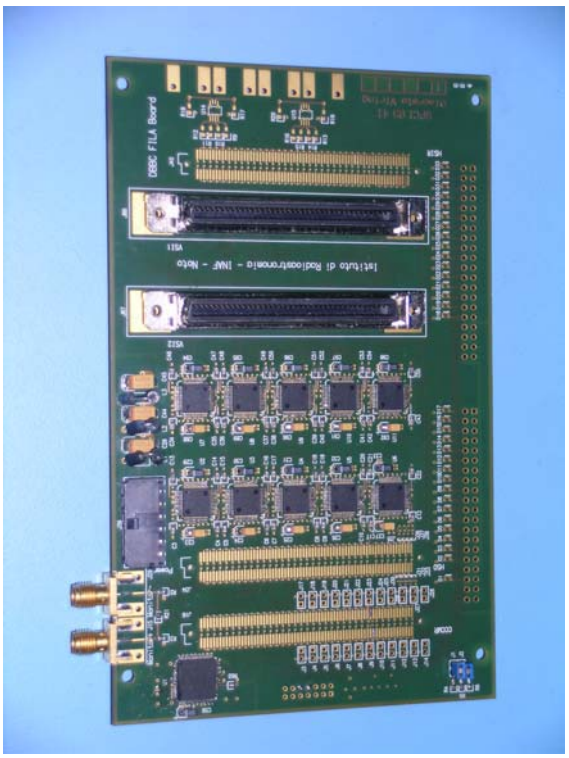

Fig. 4 The FiLa Board.

3 Upgrade

An upgrade process is under way in order to produce a new class of components to increase the performance. A description of the main elements is reported.

The ADB2 still maintaining compatibility with the ADB1 is able to sample signal up t 3.5 GHz with a sampling clock until 2.2 GHz. So the instantaneous bandwidth is up 1.1 GHz and in about three Nyquist zones the entire range can be covered. Output of this board can be slowed up to four 8-bit bus for feeding the Core processing boards. Several output modes are available depending on the clock rate adopted.

A piggy-back board can be attached to the ADB2 to extract data or inject in the sampled data chain, giving the possibility to adopt a different transfer method. In this connection the full 10-bit representation is available.

Such connection is for example used by the FiLa10G board, a second upgrade for the system. Such element is acting in a triangle connectivity in order to relate the output of the ADB2 or the input of the data samples bus with a 10Gbps bidirectional optical connection and with a set of two input and two output VSI connectors. In practice it's possible to interconnect sampled data with a 10Gbps link for a remote placement of the ADB2 and still use the same board for receiving data from a remote source. What described is a 'first stage type' functionality, but the FiLa10G is a first/last type board, so the last functionality is related to the ability to transfer processed data (coming from the last part of the chain), because VSI data can be transferred in bidirectional fashion using the optical link, so as the sampled data can be forwarded to the VSI connections. All the triangle bidirectional functionality is allowed.

The third main upgrade is related to the CoreBoard2. The new processing board is adopting a last generation FPGA device with much improved performance in terms of number of gates available and as operating clock frequency. In the down-converter functionality for instance a single CoreBoard2 is able to replace four CoreBoard1. Then the calculation density is much improved giving the additional chance to accommodate more units in a same box, with related reduction of general cost and cooling needs.

The CoreBoard2 is able, similarly to the ADB2, to support a piggy-back module, that can for example used to add a great quantity of memory to the system. This could be useful in a number of operations such as the de-dispersion functionality in the pulsar research field. Further uses can be related to a peculiar redistribution of data or correlation functions.

4 Different functionalities

With the elements described above a number of different functionalities involving a pretty variable number of input and output sources can be realized.

Three examples are described for representing the potential aspects that can be covered within the same instrument with the simple change of firmware or with the different assembly of the same parts. The first is represented by the most obvious VLBI back-end resembling the MK4/VLBA terminals. A complete system is obtained with the functionality of 8/16 independent base band converters adopting a chain as shown in the figure 5 for 8 bbcs, where a chain of a first FiLa Board, four ADBoard1, eight CoreBoard1, a last FiLa Board are placed coupled to produce a system with a maximum output data rate of 4 Gbps with two VSI connectors to supply a VSI recorder.

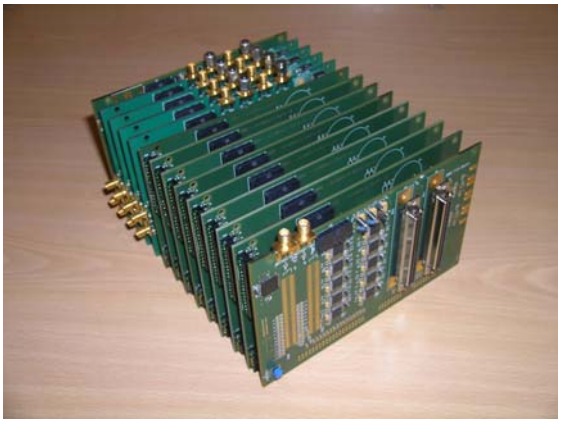

Fig. 5 System chain for a VLBA equivalent system (without conditioning Modules and PCSet).

With a simple sequence of two Fila, two ADB1, one Core1, Fila, is possible to realize a digital receiver. Such new concepts rely on the possibility to directly sample the RF signal band coming fro the front-end and, in appropriate way amplified, in order to satisfy the Conditioning Module and ADB1 requirements. MPI and IRA are developing two L-band receivers adopting this method and a direct recording is realized to produce sequence of data files to produce a direct data processing, such as VLBI cross correlation, or any other software data

reduction. Particular efforts need to be taken into account due to the fact that such system is part of the very sensitive receiver area, because placed inside the receiver body So it needs to adopt appropriate shielding methods, today under testing in MPI.

A third example is due to the multi-feed K band receiver developed in IRA that requires a general purpose backend for single-dish and VLBI operations. The system is particularly complex due to the presence of 14 different IFs (7 feeds in two polarizations). To handle the large quantity of IFs and to support the process to calculate total power in the digital domain, to realize the spectrometer functionality with 32K channels, to handle pulsar observations, to allow polarimetry measurements, etc., a sequence of a chain composed by a FiLa Board, two ADB1, one CoreBoard2, two ADB2, one CoreBoard2, ..., a FiLa Board, is adopted.

Other architectures can be assembled taking into account the needs of data processing capability and the number of input and output channels to support.

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